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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,646	08/22/2003	Guy Moshe Cohen	YOR920030328US1	8783

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,646	COHEN, GUY MOSHE	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/16/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,21-24 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,21-24 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the RCE and amendment 6/16/06.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12, 21-24, and 28-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Joshi (US006921982B2).

Joshi teaches the double-gate field effect transistor (column 10 line 4) of claims 1-12, 21-24, and 28-35 as follows.

Regarding claim 1, Joshi teaches a double-gate field effect transistor (column 10 line 4) comprising a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F).

Regarding claim 2, the channel thickness is relatively uniform (figure 8F).

Regarding claim 3, the channel material may be epitaxially grown (column 8 lines 1-4).

Regarding claim 4, Joshi forms high quality SiGe free from dislocations (column 7 lines 18-20). The examiner considers this to mean "defect free".

Regarding claim 5, the strained-silicon channel includes a distorted lattice cell. This is inherent to a strained layer.

Regarding claim 6, the gates are independently controlled (column 10 line 12).

Regarding claim 7, the strained silicon channel comprises a fin (figure 8F and column 10 line 4).

Regarding claim 8, the first and second gates are self-aligned (islands are precision aligned (column 7 lines 39-40), thus resulting gates would be self aligned.).

Regarding claim 9, the limitation of forming the first and second gates in a single lithography step is a process limitation (product by process) and has no patentable weight in device claims.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 10, the first and second gates are self-aligned as above (see claim 8) and also aligned with the source and drain, thus all are self-aligned.

Regarding claim 11, the background of the invention teaches that it is known to use one or more fins (column 1 line 42-44). Also see column 7 lines 64-65 and column 8 lines 42-43).

Regarding claim 12, the transistor includes a planarized top (figure 8F).

Regarding claim 28, the first gate is separated from the second gate (figure 8F).

Regarding claim 32, the claim is a product by process claim and the process is given no patentable weight.
Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 34, "When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be

inherent" MPEP 2112.01 1. As the structure of claim 1 is that taught by Joshi, it is inherent the same function is inherent.

Regarding claim 21, Joshi teaches a double-gate field effect transistor (column 10 line 4) comprising a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F), the strained silicon channel comprises a fin (figure 8F and column 10 line 4).

Regarding claim 22, a circuit may comprise the double-gate field effect transistor of claim 1 (column 1 lines 14-45).

Regarding claim 23, the strained silicon channel is compressively strained (column 5 line 45).

Regarding claim 24, the strained silicon channel is compressively strained (column 5 line 45 and column 6 line 66).

Regarding claim 29, the first gate is separated from the second gate (figure 8F).

Regarding claim 33, the claim is a product by process claim and the process is given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 34, "When the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent" MPEP 2112.01 1. As the structure of claim 1 is that taught by Joshi, it is inherent the same function is inherent.

Regarding claim 30, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F), and the first and second sidewalls are opposing to each other (figure 8F).

Regarding claim 31, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F) and is fixed to the substrate by the first and second gates (figure 8F).

Response to Arguments

3. Applicant's arguments filed 6/16/06 have been fully considered but they are not persuasive.

The applicant argues that the examiner has admitted that the core material 24 is not a gate and as such, Joshi only forms one gate. However, Joshi forms two gates, 88 and 89, and both sides of the channel are gated.

The applicant argues that the examiner acknowledged that Joshi does not form a double-gate Fin-FET. This is inaccurate. The examiner merely stated that the claims are not limited to a double-gate Fin-FET. Further, Joshi does form a double-gate field effect transistor (column 10 line 4).

The applicant argues that Joshi teaches a core and envelope with different lattice constants, and that the channel can have either compressive or tensile strain based upon the core material. This then reads on claim 23 (the channel is tensely strained) and 24 (the channel is compressively strained).

The applicant argues that Joshi does not teach a FinFET structure, however, Joshi does form a double-gate FinFET transistor (column 10 line 4).

The applicant again argues that Joshi does not teach a FinFET structure, as the structure includes a channel, a gate (18) over the sidewall of the envelope while the inner sidewall of the envelope is in contact with the core material, the core material not being a gate. The applicant appears to be considering figure 4. The examiner cites column 10 line 4 and figure 8F for Joshi's double-gate FinFET.

The applicant argues that there is no second gate to control the channel and that Joshi forms a single gate FET. The examiner cites column 10 line 4 and figure 8F for Joshi's double-gate FinFET with two gates 88 and 89. the examiner notes that these are device claims and the function of each gate in given no patentable weight.

The applicant argues that only one surface of the core is gated, not two. The examiner cites column 10 line 4 and figure 8F for Joshi's double-gate FinFET, two sides (surfaces) of the core being gated.

The applicant argues that Joshi shows an inverted "U" shape and this does not resemble the FinFET of the application or that defined by Hu Chenning. The examiner disagrees in that figure 8F is a double-gated FinFET, not an inverted "U" channel, and reads directly on the claims.

The applicant argues that claim 31 recites "a strained-silicon channel was elastically induced by a sacrificial stressor" and that as the stressor is sacrificial, it is not present in

the final structure and that this differs from the structure of Joshi, where the core is present in the final structure. However, the core of Joshi is part of the channel and would then be present in the final structure of the instant application. The limitation of claim 31 is a product by process limitation and given no patentable weight. The parts of the claims of the instant application are in Joshi, thus, Josh reads on the instant claims.

The applicant argues that Joshi's assertion that the SiGe is free from dislocation ids incorrect as the laws of physics do not enable SiGe to relax without forming defects. The applicant points to cited art provided by the applicant on 11/8/05. However, Joshi asserts the SiGe is relaxed and free from dislocation. the applicant would need proof, not argument that Joshi could not, under any circumstance within the context of his teaching, form a SiGe layer free from dislocations. Otherwise, the examiner must rely on Joshi's assertion. Previously, the applicant argued that Joshi does claim that the SiGe is free from dislocation, but to the inventor's knowledge, experimental data does not support this claim. However, the patent, by law, is considered enabled. Arguments are not considered in this matter. Conclusive proof would be necessary to show that the claim of Joshi is not enabled. The applicant has not provided conclusive proof, only argument.

The applicant argues that dependent claims 34 and 35 define the double gate and Joshi is devoid of such teaching. However, the examiner cites column 10 line 4 and figure 8F for Joshi's double-gate FinFET.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

July 3, 2006